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NSTX PRINCETON PLASMA PHYSICS LABORATORY

1903 1 MS CAMAC Memory Board
General Requirements Specification

A-AEXXXX

SHT 1 OF 13

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Tables and Figures

Abstract

This specification, in conjunction with referenced documents, sets forth all characteristics of subject module. The intended use of this document is to provide a minimum design goal for the module, as well as a working document for subsequent users.

Reference Documents

IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), IEEE Std. 583-1975.

CAMAC – A Modular Instrumentation system for Data Handling. AEC TID-25875.

Printed Circuit Board Fabrication and Assembly Specification, Document No. TFTR-10A2-H54.

Electronic Schematic Specification, Document No. TFTR-10A2-H55.

Printed Circuit Artwork Specification, Document No. TFTR-10A2-H53.

Reliability, Quality Control and Temperature Cycling, Document No. TFTR-10A2-H58.

Plug-In-Unit(36 Aux), Document No. PG-001-01.

Transient Digitizer, Document No. TFTR-10C6-H908.

Generic Standard on Printed Board Design, IPC Std. No. IPC-2221A.

Sectional Design Standard for Rigid Organic Printed Boards, IPC Std. No. IPC-2222A.

Introduction

The CAMAC module specified will be used as an interface between elements of the National Spherical Tokomak Experiment (NSTX). The module will be housed in a standard CAMAC crate. The module will function as a 1M word (1x10^6 words) memory to be used in conjunction with a high - speed analog to digital converter module.

Basic Features

The module shall be a single width CAMAC module that will provide solid state memory for 1M data words up to 12 bits wide. The memory will be loaded and unloaded through the use of the rear 36 conductor auxiliary connector. Dataway utilization will be limited to only providing DC power for the modules’ low dropout power regulators. The memory will be fully compatible with the CAMAC Transient Digitizer. The memory shall provide full 20 bit address decoding.

Mechanical Characteristics

The module shall conform to mechanical specifications as indicated in PG-001-01, as this module will contain the 36 conductor auxiliary edge connector.

The module shall be a single (1x) width CAMAC module.

The electrical components of this module are to be mounted on a high quality, flame retardant, glass - epoxy substrate, such as Rodgers FR-4, Isola copper - clad laminate/prepreg type material or other type of equivalent as necessary.

This module is to contain all necessary mechanical components for insertion into a standard CAMAC crate.

All components are to be identified with a silkscreen reference designator (unless inappropriate to place near the component) near, or appropriately close to, the component. Reference designators shall parlay to a standard bill of materials (BOM)/parts list where the components part number, manufacturer, and other pertinent information can be obtained.

The operating condition of this module is to be monitored by LED’s located on the module’s front panel. All lettering on said front panel shall be engraved or silkscreened. The front panel

material shall be aluminum, with an iridite finish and contrasting colored lettering.

The rear 36 conductor auxiliary edge connector shall be used for connection to the Transient Digitizer and other memory modules as well. Pin assignments and net names shall conform to table 1.

Electrical Characteristics

The dataway interface shall conform to the specification as indicated in the references in the front.

Input power shall be derived from the standard +6 VDC CAMAC power supply voltage. Low – power circuitry will be used throughout this device. All input DC power traces shall be of sufficient width, guarding, and be fitted with an appropriately sized through – hole fuse. The maximum total power dissipation (P_{diss}) shall not surpass **<X Watts>** from all voltage sources.

The +6 VDC supply line will be bypassed on the module with high quality, surface mount tantalum capacitors of at least 33 microfarads and very low ESR (Equivalent Series Resistance). The +24 VDC and -24 VDC supply lines will also be bypassed with high quality, through – hole aluminum electrolytic capacitors of at least 220 microfarads and be rated for a DC voltage of at least 25 volts. In addition, each integrated circuit will be placed

near a 0.1 microfarad, through – hole, Multi - layer Ceramic (MLCC) bypass capacitor. For TTL devices, this capacitor shall have a DC voltage rating of at least 6V, while bypass capacitors placed near CMOS devices shall have a DC voltage rating of at least 5V. As per standard PCB design practice, these capacitors will be placed as close to the devices power pins as possible.

The module will use tri – state devices for the data bus (DB) lines and hysteresis type line receivers for the address bus (MAB) and read and write strobe lines.

The module shall function as a remote static random access memory (SRAM) unit. If dynamic RAM (DRAM) components are used, all refresh cycles shall be internal to the board circuitry and be transparent to the user. Additionally, if dynamic RAM components are used, error correcting circuitry (ECC) shall be included for correction for any single bit upset per 12 bit data word.

The module timing shall be designed to accommodate a maximum loading rate of **<insert loading rate>** words per second and a maximum unloading rate of **<insert maximum unloading rate>** words per second. Typical unloading parameters are suggested in this document. The vendor of the memory modules shall provide

detailed timing diagrams and parameters for incorporation into this specification.

The module will provide 2 LED indicators mounted on the front panel, and will be triggered as follows:

- LED #1 (Load): To be illuminated for approximately 50 milliseconds whenever the module is addressed and is loading.
- LED #2 (Unload): To be illuminated for approximately 50 milliseconds whenever the module is addressed and is unloading.

Environmental Data

The module must operate, as defined, over an ambient temperature range of 0°C - +50°C.

The module must operate, as defined, over a relative humidity range of 10% - 90%. It is not a requirement that the module operate under conditions of water condensation.

The module must operate, as defined, in the presence of an external magnetic field, changing at the rate of (100 Gauss/sec), with a peak magnitude of 200 Gauss in any direction.

The module must operate, as defined, in a radiation environment as follows:

- **Neutrons: ?**
- **Radiation – Dose: ?**
- **Integrated Dose: ?**

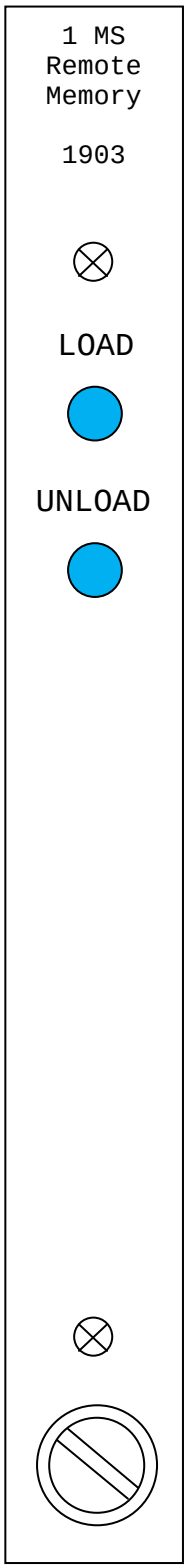
Safety

All components of this module must be of modern flame retardant material.

All materials, including the device’s final solder profile, must be free of lead (Lead – Free, Pb – Free, etc.) and conform to all current EPA and IPC environmental standards and initiatives (RoHS – Reduction of Hazardous Substances, etc.). Integrated circuit and passive component lead free certifications should be kept on record in case of inquiry.

Testing

The module will be subjected to rigorous manufacturing quality and functional tests throughout its various states of development, culminating in a final test of all functions prior to final delivery. A description of these checks and tests will be documented in a formal test plan to be submitted along with all other final documentation upon delivery.



Note: Not drawn to scale

Figure 1: Front Panel Layout

Component (Left) Side (Side B)		Bottom (Right) Side (Side A)	
Pin	**Function**	**Pin**	**Function**
1B	MAB 19	**1A**	MAB 1
2B	MAB 18	**2A**	MAB 0
3B	MAB 17	**3A**	GND
4B	MAB 16	**4A**	DB 11
5B	MAB 15	**5A**	DB 10
6B	MAB 14	**6A**	DB 9
7B	MAB 13	**7A**	DB 8
8B	MAB 12	**8A**	DB 7
9B	MAB 11	**9A**	DB 6
10B	MAB 10	**10A**	DB 5
11B	MAB 9	**11A**	DB 4
12B	MAB 8	**12A**	DB 3
13B	MAB 7	**13A**	DB 2
14B	MAB 6	**14A**	DB 1
15B	MAB 5	**15A**	DB 0
16B	MAB 4	**16A**	GND
17B	MAB 3	**17A**	Write Strobe
18B	MAB 2	**18A**	Read Strobe

Table 1: Auxiliary Connector Pin Assignments

Note: Table corresponds with “front of crate” viewing.

Typical Timing Diagrams

<Memory Module Timing diagrams to be inserted here TBD.>

Figure 2: Read Cycle

Figure 3: Write Cycle

Switching Characteristics

For Read Cycle:

Parameter	Symbol	Minimum	Maximum	Unit
Read Cycle Time	t_{RC}	55	-	ns

Table 2: Read Cycle Timing Characteristics

For Write Cycle:

Parameter	Symbol	Minimum	Maximum	Unit
Write Cycle Time	t_{WC}	55	-	ns

Table 3: Write Cycle Timing Characteristics